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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,161	08/21/2003	John A. Geen	2550/182	7607

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Steven G. Saunders
Bromberg & Sunstein LLP
125 Summer Street
Boston, MA 02110-1618

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,161	GEEN, JOHN A.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Aug 21 & Sep 30, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08212003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 7 and 20 are objected to because of the following informalities: Since one of ordinary skill in the art would understand the first stage does not have an "immediately preceding stage", it is suggested the "each stage" phrase be changed to --each stage, after the first stage,-- in claims 7 (lines 3-4) and 20 (line 4). This change will minimize possible confusion by more clearly implying the frequency of the first stage will be the base frequency. For example, if the frequency of the first stage is f, then the frequency of the second stage will be either 2f or f/2, which is double or half the frequency of the second stage's immediately preceding stage (i.e. the first stage). Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is believed the series connection of the series pair "between the input voltage and ground" in claim 12 is inaccurate. With this type of configuration, the input voltage will be shared across the two capacitance, wherein each capacitance will be half the input voltage (assuming the capacitances are the same size). This would divide the input voltage instead of allowing it to be multiplied or summed. Was the series pair meant to be coupled between the input voltage and the output (instead of ground)?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11, and 13-20 are rejected, and in so far as being understood claim 12 is also rejected, under 35 U.S.C. 102(b) as being anticipated by Imi. Fig. 1 of Imi shows a voltage multiplier comprising first stage D_1,C_1,S_1,S_2 having an input (i.e. common connection of D_1,S_1) receiving input voltage Vcc; and second stage D_2,C_2,S_3,S_4,C_0 in series with the first stage, and having an input (i.e. common connection of D_2,S_3) for receiving the first stage output voltage (i.e. from common connection of D_1,C_1). From the disclosure (e.g. see column 5, lines 17 and 29), it is understand each stage is capable of multiplying its respective input voltage by an amount (e.g. 2.0) to produce its respective output voltage. Since Fig. 1 shows only two stages, its final output voltage V_{DD} will be equal to 4xVcc (i.e. see column 5, lines 38-46), and claims 1-2 are anticipated. First stage D_1,C_1,S_1,S_2 and second stage D_2,C_2,S_3,S_4,C_0 have first/second capacitances C_1/C_2, respectively, wherein the second stage also has output capacitance C_0. Using Fig. 2(F) as a reference, it would be understood output capacitance C_0 is periodically charged to the second stage output voltage C_{2+} (i.e. 4Vcc) about twenty-five percent of the total time, thus anticipating claim 3. Between Figs. 1 and 2, it is understood the first stage has a switching speed that is half the switching speed of the second stage (e.g. see Figs. 2(A)-2(B) versus Figs. 2(C)-2(D)). Since the first switching speed (with respect to S_1,S_2) is a function (e.g. half) of the second switching speed (with respect to S_3,S_4), claims 4-5 are anticipated. Fig. 7 shows voltage

multiplier having first stage D_1,C_1,S_{1A},S_{2B}; second stage D_2C_2,S_{2A},S_{2B}; and a plurality of additional stages (i.e. D_3,C_3,S_{3A},S_{3B} and $D_N,C_N,S_{NA},S_{NB},C_0$) coupled in series with the second stage. The final stage $D_N,C_N,S_{NA},S_{NB},C_0$ produces final output voltage V_{DD} that is the product of input voltage Vcc and 2.0 to the Nth power, where N equals the number of stages (i.e. first – final stages). For example, see column 6, lines 48-54. Therefore, claim 6 is anticipated. Similar to Figs. 1-2, each stage shown in Fig. 7 has its own respective capacitor that is switched between different nodes based on a base frequency. Since first stage stage D_1,C_1,S_{1A},S_{2B} does not have any "immediately preceding stage", its switching speed is considered the base frequency, wherein the other stages each have a switching frequency that is twice or half that of the immediately preceding stage, anticipating claim 7. For example, see column 6, lines 55-61. Final stage $D_N,C_N,S_{NA},S_{NB},C_0$ also has output capacitor C_0 for providing output voltage V_{DD} for that stage, wherein that output voltage is greater than the output voltage of each preceding stage, thus anticipating claim 8. Referring now to Fig. 9, which replaces diodes D_1,D_2 of Fig. 1 with switches S_7,S_8, respectively (e.g. see column 7, lines 14-22), one of ordinary skill in the art would understand that when S_7,S_2, are closed and S_1, is open, first capacitance C_1 will be coupled between input voltage Vcc and ground, thus causing the first capacitance to be charged to be substantially equal to input voltage Vcc; with switches S_7,S_2,S_3 opened, and switches S_1,S_8,S_4 closed, the first capacitance will be coupled to second capacitance C_2 to charge the second capacitance to a second voltage 2Vcc (e.g. see column 5, lines 6-8) which is substantially equal to the sum of input voltage Vcc and the voltage (e.g. substantially equal to input voltage Vcc) of the first capacitance; and when the switches are configured to couple the first/second capacitances in series between Vcc and output node V_{DD}, output voltage V_{DD} (i.e. 4Vcc – see

column 5, lines 37) will be substantially equal to the sum of the input voltage and the voltage across the first/second capacitances, anticipating claims 9 and 13. Due to the operation of their respective switches, the first/second capacitances are uncoupled and re-coupled to produce output voltage V_{DD}. For example, first capacitance C_1 is periodically coupled between input voltage Vcc and ground to recharge the voltage (e.g. Vcc) across the first capacitance; second capacitance C_2 is periodically coupled between the output voltage (e.g. Vcc) of the first stage/ capacitance and ground to recharge the voltage (e.g. 2Vcc) across the second capacitance; and first/second capacitances C_1,C_2 are periodically coupled in series between input voltage Vcc and the output to produce output voltage V_{DD}. These uncoupling and re-coupling operations anticipate claims 10 and 12. Output capacitance C_0, coupled to the output node, anticipates claim 11. As shown and understood from related Figs. 2(A)-2(D), and the disclosure (e.g. see column 6, lines 55-60), the first switching frequency is one of double or half the second switching frequency, anticipating claim 14. By re-identifying the previously described first stage D_1,C_1,S_1,S_2; second stage D_2,C_2,S_3,S_4,(C_0); first/second capacitances C_1/C_2; output capacitance C_0; and plurality of additional stages as first multiplying means, second multiplying means; first/second capacitance means, output capacitance means, and plurality of additional multiplying means, respectively, claims 15-20 are anticipated for the same reasons as previously described above with respect to claims 1-7.

No claim is allowable.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although not used in any formal rejections

described above, each of the references could have been used to reject at least claims 1-2, 6, 8, 15-16, and 19; and the Yatabe reference could also have been used to reject claims 9-13. Each reference shows a plurality of multiplying stages coupled in series, wherein each stage is capable of having a multiplying amount of 2.0. For example, see Cernea (Figs. 3-4), and Yatabe (Figs. 10-11). Therefore, these references should be carefully reviewed and considered.

The prior art reference submitted on Aug 21, 2003 was reviewed and considered. The reference shows and discloses preferred capacitive voltage multipliers, including the use of an output capacitor coupled to the output of the multiplier to maintain a constant voltage at the output. However, the reference does not clearly show or disclose the plurality of multiplier stages coupled in series, wherein each stages has its own respective switching speed (e.g. frequency) that differs from the other stage(s).

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund

25 August 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800